## Notice of References Cited Application/Control No. 10/731,593 Applicant(s)/Patent Under Reexamination BAECKLER, GREGG Examiner Suzanne Lo Art Unit Page 1 of 1

## U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-7,020,864	03-2006	Loong, Low Yau	716/16
*	В	US-7,020,855	03-2006	Wallace, David E	716/2
*	С	US-5,748,488	05-1998	Gregory et al.	716/18
*	D	US-6,086,626	07-2000	Jain et al.	716/5
*	Е	US-6,026,230	02-2000	Lin et al.	703/13
*	F	US-6,195,788	02-2001	Leaver et al.	716/18
*	G	US-6,990,650	01-2006	Teig et al.	716/12
	Н	US-			
	1	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-		·	

## FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	·				
	0					
	Р					
	Q					
	R			· · · · · · · · · · · · · · · · · · ·		
	s					
	Т					

## NON-PATENT DOCUMENTS

*	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)					
	υ	Lee et al. "Performance evaluation and optimal design for FPGA-based digit-serial DSP functions", 11/15/02, Science Direct, http://www.sciencedirect.com, 21 pages				
	٧	Vemuri et al. "BDD-Based Logic Synthesis for LUT-Based FPGAs", October 2002, ACM Transactions on Design Automation of Electronic Systems, Vol. 7, No. 4, Pages 501-525.				
	w					
	x					

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.